REMARKS

Claims pending in the present patent application are numbered 1, 3 and 6-8. Claims 2, 4, 5 and 9-15 were previously canceled. The rejections set forth in the Office Action dated July 13, 2006, have been carefully considered by the Applicant. Applicants respectfully assert that the pending Claims are in condition for allowance.

103 Rejection

Claims 1, 3 and 6-8 are rejected under 35 U.S.C. 102 as being anticipated by Tanaka (US Patent No. 6,756,675; hereinafter "Tanaka") in view of Heim (US Patent No. 5,248,903). Applicants have reviewed the cited reference and respectfully submit that the embodiments of the claimed invention that are set forth in Claims 1, 3 and 6-8 are not anticipated or rendered obvious by Tanaka in view of Heim.

The Examiner is respectfully directed to independent Claim 1 which is drawn to a semiconductor device. Claim 1 is reproduced in it's entirety below for convenience of the Examiner.

> A semiconductor device comprising:
> a pad metal layer having a perimeter area and a center area;
> a lower metal layer having a plurality of apertures below said center area of said pad metal layer, wherein said apertures are arranged into a plurality of rows each row comprising more than one of said apertures and a plurality of columns each column comprising more than one of said apertures;
> an interlayer dielectric formed between said pad metal layer and said lower metal layer;
> a plurality of vias formed in said interlayer dielectric, wherein said vias electrically couple said pad metal layer and said lower metal layer, and wherein said vias form a ring arrangement only below said perimeter area of said pad metal layer; and
> an insulating dielectric layer that covers said perimeter area of said pad metal layer. (emphasis added)

Claims 3 and 6-8 depend from Claim 1 and set forth additional limitations of the claimed invention.

Tanaka in view of Heim does not anticipate the embodiments of the invention as set forth in Claims. Tanaka does not teach or suggest all of the limitations of the claimed embodiments and Heim does not remedy the deficiencies of Heim. In particular Tanaka does not teach or suggest a semiconductor device that features a plurality to of vias that "form a ring arrangement only below said perimeter area of said pad metal layer" as is set forth in Claims. And, Heim does not teach this limitation to remedy the deficiencies of Tanaka. Moreover, the limitation purported by the Examiner as being taught by Tanaka actually would destroy a basic principle of the design of Tanaka.

Tanaka shows a dissimilar semiconductor device that includes a connecting region for an external connecting terminal. Importantly, in the Tanaka device the disclosed connecting system is very different from the connecting system employed in the embodiment of the claimed invention that is set forth in Claim 1. In Figures 1-9B and the corresponding text, Tanaka teaches a semiconductor device having a pad metal layer 100 positioned over a lower pad metal layer 200, wherein the lower metal layer 200 has a plurality of apertures 130a-130g. Moreover, Tanaka teaches an insulating layer 150 between the pad 100 and lower 200 metal layers. Tanaka also teaches a plurality of vias 110a-120d connecting the pad 100 and lower 200 metal layers.

Importantly, In Figures 1, 2A, 6A, 7A, 8 and 9A Tanaka teaches that the plurality of vias connecting the pad 100 and lower 200 metal layers are positioned throughout the

insulating layer 150. This is very different from the embodiment of the invention that is set forth in Claim 1 which includes "a plurality of vias formed in said interlayer dielectric, wherein said vias electrically couple said pad metal layer and said lower metal layer, and wherein said vias form a ring arrangement only below said perimeter area of said pad metal layer." Tanaka fails to teach or suggest the ring arrangement of vias located only below the perimeter area recited in Claim 1.

Heim does not teach or suggest a modification of Tanaka that that would remedy the deficiencies of Heim noted above. In particular, Heim does not teach or suggest a semiconductor device that features a plurality of vias that "form a ring arrangement only below said perimeter area" of a pad metal layer as is set forth in Claim 1, that can be combined with Tanaka. Heim shows a dissimilar bond pad scheme for semiconductor devices. The scheme disclosed by Heim is dissimilar from that which is set forth in the claimed embodiments as the scheme disclosed by Heim does not include features such as the recited lower metal pad having apertures below a center area. Moreover, as alluded to above, the scheme disclosed by Heim is incompatible with that of Tanaka as it would destroy a basic principle of the design of Tanaka. The Examiner contends that Heim discloses the use of vias in a peripheral area of metal layer. However, because Tanaka already teaches that structures are located in this area of his device (see conductive members 110 in Figure 1), modifying Tanaka to include such peripheral vias would destroy a basic operating principle of the Tanaka design. Combining references where a basic principle of the design of the primary reference is destroyed is impermissible under US Patent Law (see MPEP 2143.01). Consequently, the embodiments of the invention as

set forth in Claim 1 (Claims 3 and 5-8 depend from Claim 1) are not anticipated or rendered obvious by Tanaka in view of Heim.

Therefore, Applicants respectfully submit that the rejection of Claim 1 under 35 U.S.C. §103 is improper and that Claim 1 is in condition for allowance. Accordingly, Applicants respectfully submit that Claims 3 and 6-8 dependent on Claim 1 are likewise in condition for allowance.

CONCLUSION

Applicants respectfully submit that all remaining claims are neither anticipated by nor rendered obvious in view of the cited references. For at least the above-presented reasons, it is respectfully submitted that all remaining claims are in condition for allowance.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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Date: 9/27/06

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